PFC Single Conversion Line Ripple Cancellation Using the Yeaman Topology

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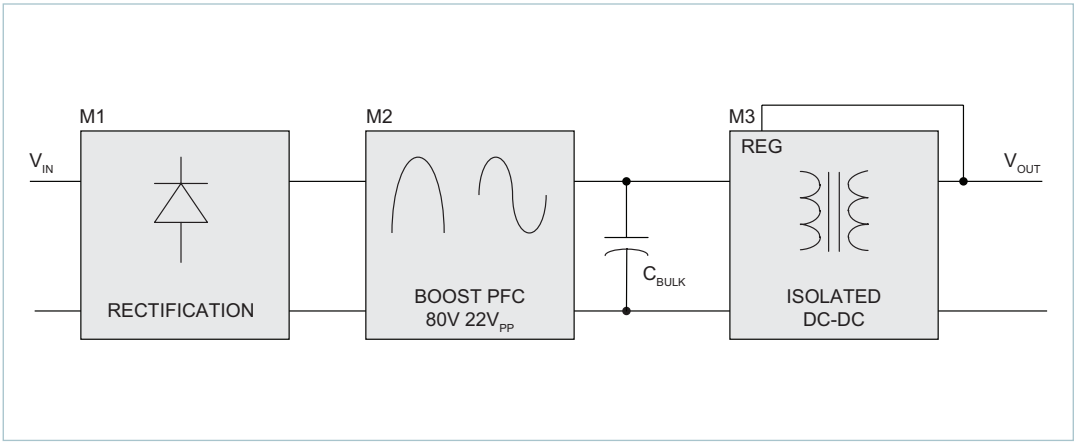
Abstract

This paper introduces a new application of the previously introduced "Yeaman Topology". [a] The main characteristic of this topology is to separate the output voltage regulation function from the bulk power-conversion function, as it is used in DC-DC converters. Usage with single-conversion PFC AC to DC converters confers the ability to efficiently regulate the line ripple on the output bus by over two orders of magnitude without needing to reprocess 100% of the energy coming from the previous conversion stage. The result is in an increase of power density, efficiency and lower cost than a traditional post-processing stage.

Single-stage PFC vs. two-stage PFC converter characteristics

Most PFC converters on the market are two-stage converters. A typical block diagram looks like Figure 1 below:

Figure 1
Block diagram of a typical two-stage PFC AC-DC Converter

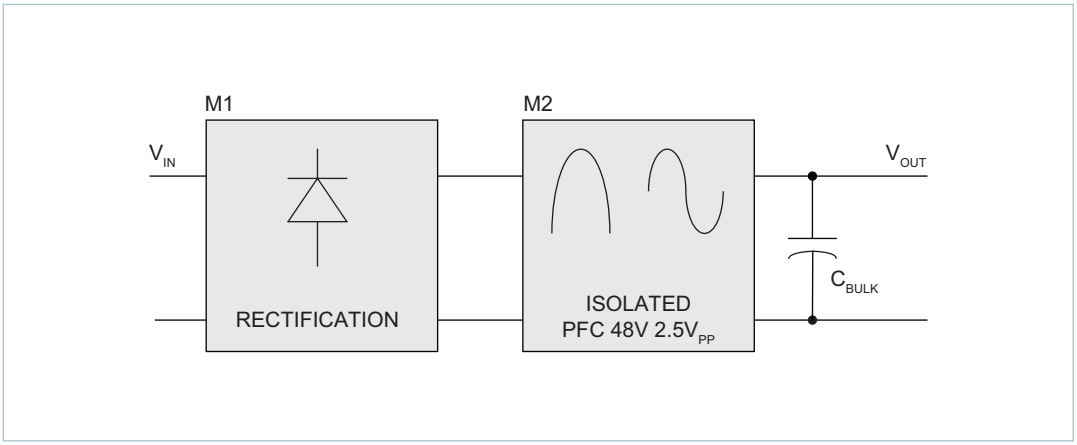


The relevant characteristics for the purposes of this paper is that M2 is controlled solely to obtain a high power factor, which results in a ripple voltage on C_{BULK} at twice the input line frequency. This ripple voltage cannot be avoided, as the input current shape is required to follow the 50 or 60Hz sine wave shape at the input. M3 is added to the output to convert the high voltage to a usable lower voltage, provide galvanic isolation and regulate the output voltage so that the 100 or 120Hz line ripple seen on the bulk capacitor is not presented to the load at V_{OUT}.

Vicor makes a single-stage isolated 330W power factor-corrected converter that converts a universal 90 – 264V_{RMS} input voltage in a single stage, directly to +48V. [b]

The single conversion stage can perform PFC, galvanic isolation and transformation down to +48V, shown in Figure 2:

Figure 2
Block diagram of a Vicor single-stage PFC AC-DC Converter

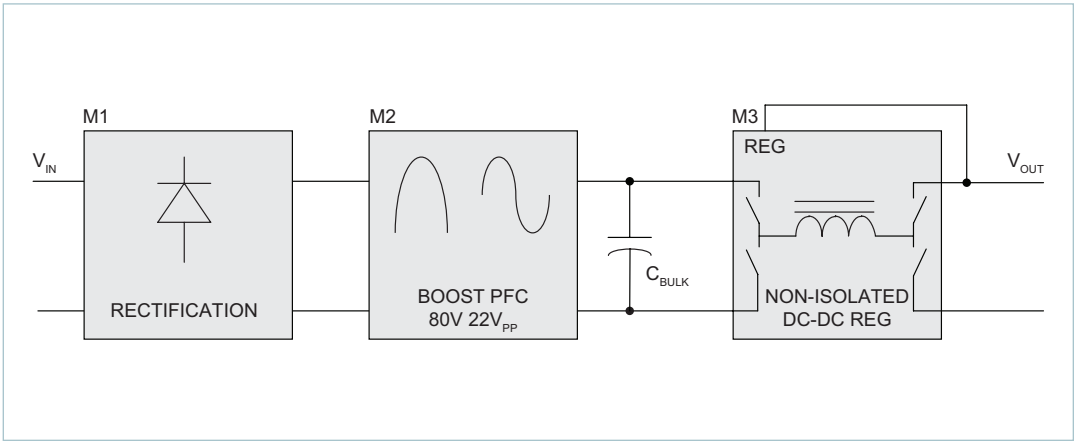


The PFC bulk-storage capacitor is in the SELV region of the circuit, has small safety spacing requirements and can be intermixed with other SELV circuits in the customer's circuit.

One of the challenges it creates, however, is the relatively high output ripple voltage at twice the line frequency that is created by the PFC action of the converter. With the bulk capacitor scaled for same hold-up energy, the output ripple will be lowered a factor of 48/380V lower, but the same in terms of percentage of nominal output voltage.

When used in the primary intended application, feeding downstream point-of-load converters, this higher ripple is inconsequential. There is a desire to create a regulated higher-voltage bus in some applications, where the high circuit density and ease of use of the single-stage converter is desired. The obvious solution is a following post regulator stage [c], shown in Figure 3 below:

Figure 3
Block diagram of a Vicor single-stage PFC with post regulator



Some of the advantages claimed by a single stage of PFC conversion have been lost. Density and efficiency have been reduced due to the addition of this second stage of conversion. While the non-isolated DC-DC regulator is a high-efficiency buck-boost standard module, the isolated PFC converter does not have as good efficiency as the boost PFC shown in Figure 1, so the net result is not as good as desired.

This paper introduces a different solution, which we have called the Yeaman Topology. It helps to alleviate some of the shortcomings of the follow-on post-regulator M3.

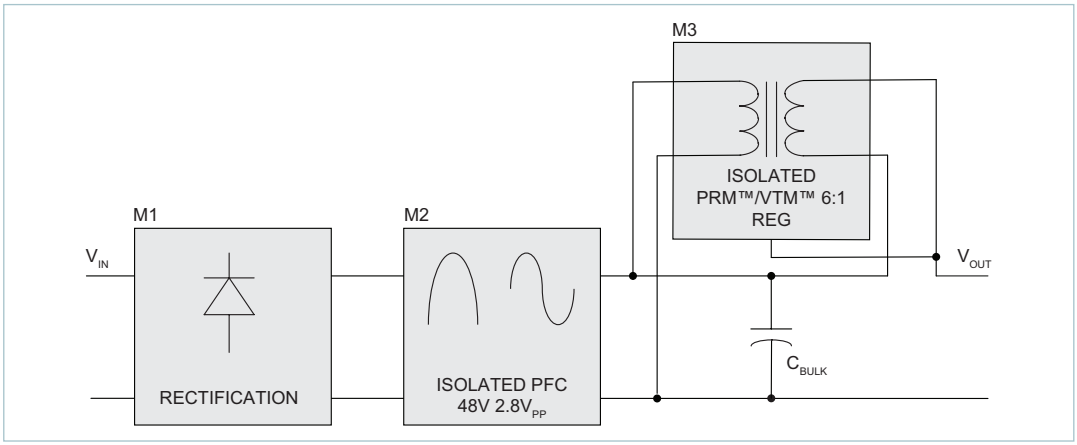
Introduction of the Yeaman Topology

The Yeaman Topology has been previously introduced for use in DC-DC power conversion systems.[a] It involves the formation of an output using a series combination of DC-DC converters, taking advantage of the isolation to put the outputs in a series stack. One converter is typically a high-efficiency fixed-ratio bus converter with no feedback, while the other is a lower efficiency regulating stage that is capable of regulated the output over the entire range of operation that is powered by both stages.

The intended result is that most of the power is provided by the less costly, more efficient converter, while the regulation is handled by a converter that handles a small fraction of the output load, such that the detrimental effect on cost and efficiency has a smaller impact on the overall converter design than if the converter used a single up-scaled regulated stage.

This idea is presented in the block diagram shown in Figure 4:

Figure 4
Single-stage AC-DC converter with Yeaman Topology



This configuration of Yeaman Topology differs from that in [a] in that the unregulated bus converter has been replaced with the single-stage PFC converter. The regulation shortcoming due to the fixed-ratio bus converter has been replaced by the need to regulate the output ripple at twice line input line frequency. One other difference should be noted regarding the input of the supplemental converter. Because an AC-DC converter needs to handle a rougher interface, including lightning strikes on the input, the supplemental converter that forms the Yeaman Topology is powered by the output of the single-stage PFC converter rather than the input.

The concept is the same as in the DC-DC converter case. The output is fed back so that M3 drives V_{OUT} to $54V_{DC}$, trying to reject the ripple present at the output of M2. The second smaller, better regulating output stage is stacked in series with the primary converter, with the expected result of a more efficient system than a post regulator.

Correct sizing of Yeaman Topology converter components

Since the power stages of M2 and M3 are connected in series, their powertrains deliver the same current. The output power ratio will equal the output voltage ratio of converters M3 and M2.

The output voltage of M3 must be large enough to handle the output ripple voltage of M2, half of which swings above and half of which swings below the average bus voltage. C_{BULK} controls the output voltage ripple and can be traded off to reduce system cost or to increase system density. In practical commercial systems, however, it is generally the lowest capacitance that can support hold-up requirement to supply energy to the load during a short input interruption, in some cases for volume reduction rather than for cost reasons.

The ripple current of M2 is generally a fixed percentage of the load current, although the amplitude needs to be adjusted for dead time near zero crossing for our converter. For M2, this can be approximated by Equation 1:

$$V_{BULK\_PP} = \frac{1.13 \bullet I_{OUT\_DC}}{2\pi \bullet f_{LINE} \bullet C_{BULK}} \qquad (1)$$

If M3 is a single-quadrant power supply, it needs to have an output voltage that can be adjusted with a range at least as large as the ripple voltage on the bulk capacitors, plus some margin to account for tolerance stack up through all operating ranges of the converter. For this case study, a 48V 330W PFC AC-DC converter with 4.0V_{PP} line ripple was fitted with an auxiliary power supply to form a 54V 300W regulated output.

Because the two supplies in the Yeaman Topology are in series, the power rating of the supplies should be scaled by the ratio of the output voltages. Because M3 provides only a fraction of the output power, V_{M3}/V_{M2}, only that fraction of the output suffers the loss in efficiency due to double conversion.

$$P_{OUT} = (V_{M2} + V_{M3}) \bullet I_{OUT} \qquad (2)$$

$$P_{IN} = \frac{V_{M2} \bullet I_{OUT}}{\eta_2} + \frac{V_{M3} \bullet I_{OUT}}{\eta_2 \bullet \eta_3} \qquad (3)$$

$$\eta_{2,3} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{M2} + V_{M3}}{\frac{V_{M2}}{\eta_2} + \frac{V_{M3}}{\eta_2 \bullet \eta_3}} \qquad (4)$$

It can be further seen in Equation 4, as V_{M3} becomes smaller compared to V_{M2}, the efficiency of the combined system approaches η_2. If M3 is a two-quadrant power supply, that can process power in either direction, you will be close to that limit. The losses that apply to handling the ripple current, which had intentionally been neglected as part of the simplification, will dominate the additional loss expended for regulation.

Supplemental Converter Implementation

Vicor has an extensive line of power modules that are packaged to be as easy to use as op-amps. Two units have been chosen to implement the supplemental converter, the PRM™ [c] module and the VTM™ [d] module. Both devices are optimized to work with a 48V_{DC} input.

The PRM (Pre-Regulator Module) that uses a buck-boost topology to either buck or boost the input voltage. It is being used in a remote-sense configuration that allows an external input for feedback. The part chosen is a PRM48AH480T200A00, which can deliver 200W in 22 x 16.5 x 6.73mm package. The efficiency of this part is best when the output voltage is near the input voltage; however we also need to be mindful of the minimum and maximum voltage ranges needed to stay within regulation.

The PRM does not provide galvanic isolation, which is needed to stack the output. This is provided by another Vicor module, the VTM (Voltage Transformation Module). This module acts like a transformer that can work on DC inputs. It has been optimized to work with a PRM driving its inputs and is available in different turns ratios.

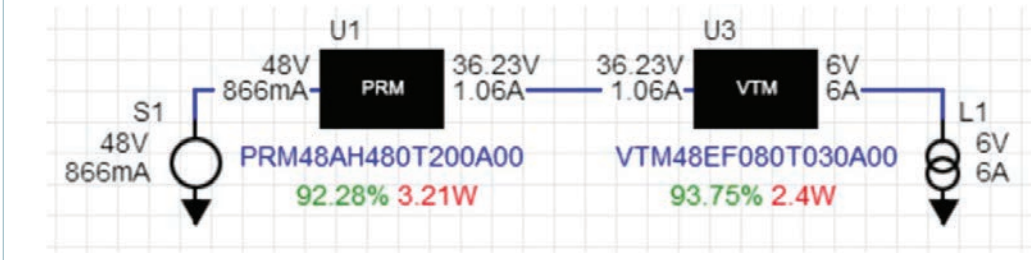
The maximum PRM output voltage is 55V. The minimum expected PFM output will vary based on whether only the ripple is to be cancelled or if we wish to boost the output in the event for a line dropout. For this exercise, assume we are interested only in the former and that we wish to be able to regulate the output when the minimum output is 46V. For an output of 9V, the VTM needs to have a turns ratio of 55/9, roughly 6:1.

Vicor part number VTM48EF080T030A00 is a full-sized chip, 32.5 x 22 x 6.73mm, capable of 30A output. A half-sized chip would be a better choice, but it is not available in this turns ratio.

At nominal inputs, it will be boosting 48V from the PFM to 54V, 6V_{OUT}. The nominal value for the PRM output will therefore be 36V.

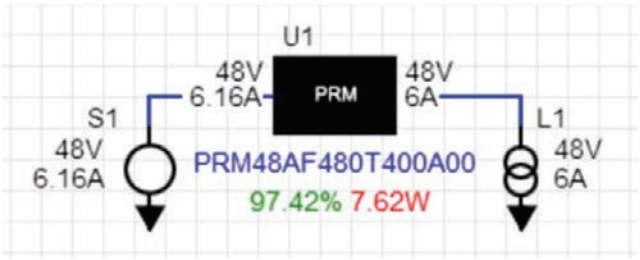
Vicor has a web-based tool that can be used to verify voltage, current and power ranges and estimate power losses, called the PowerBench™ whiteboard, [e] shown in Figure 5. Using the nominal output of 324W at 54V for the stacked supply, the load current of 6A and 6V are plugged into the model. The tool interpolates expected losses based on temperature compoensated test data.

Figure 5
Efficiency calculation, Vicor PowerBench™ whiteboard for supplemental converter



Returning back to the alternative presented in Figure 3, we can use the same Whiteboard tool to calculate the losses using the PRM™ as a post regulator, without the need of the VTM™. The PRM must be swapped out with a larger one that can handle 324W of output power.

Figure 6
Efficiency calculation, Vicor PowerBench™ whiteboard for post-regulating converter



The original point of the Yeaman Topology with respect to efficiency has hit a problem. The supplemental converters shown in Figure 5 are handling only 36W, yet they are capable of 200W. This low in the power handling capability, their efficiency has dropped quite far from the high 90% figures that these converters can reach. This is due to the fact that parts used were the most convenient, rather than the ones best suited to the task.

Even with that setback, with the composite efficiency only 86.51%, the supplemental converter only processes 11% of the output power. Only 5.61W is dissipated.

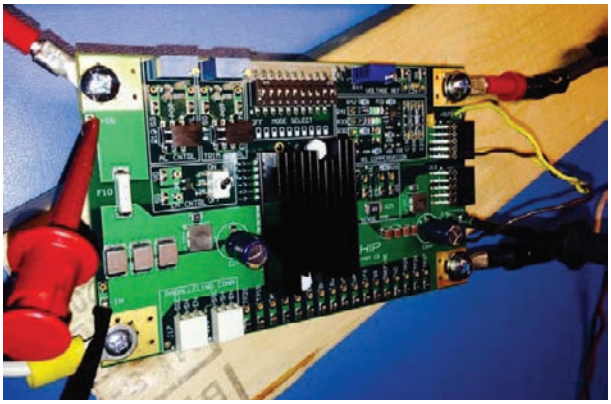
In contrast, the higher-efficiency post regulator operates at 97.42% efficiency, but needs to process all 300W of output power, so that 7.62W is lost.

Had lower-power parts been used for the supplemental converter, or a larger output power been required, the expected benefit would have been larger.

Experimental Verification

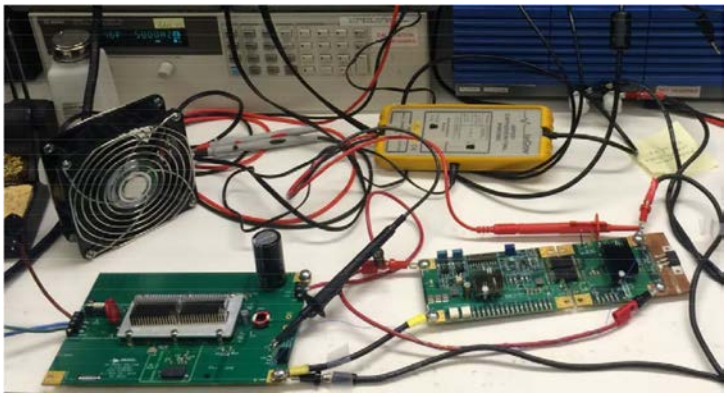
All three components used are available on evaluation boards, such as shown in Figure 7. The boards were ordered, connected and tested to measure performance.

Figure 7
PRM evaluation board, with local loopback to external-sense differential amplifier



First we measured the efficiency in the post-regulator configuration. We then reconnected the modules in the Yeaman Topology, shown in Figure 8:

Figure 8
Experimental Yeaman Topology circuit, with PFM™, PRM™ and VTM™ modules (left to right)



Efficiency comparison is in Table 1. Data is presented side by side for the post-regulated output and the Yeaman Topology output, for 120V 60Hz and 240V 50Hz data. In addition, data are presented for 163W and 325W output.

Since the output is held constant for all the test cases, efficiency can most easily be compared by comparing input power to the system. These values have been highlighted with bold text. Although the benefit is reduced at half output power, the Yeaman Topology input power is lower in every test case. The system efficiency percentages listed at the bottom show the same results as we have seen above for the theoretical case, that although the supplemental converter M3 has poor efficiency due to low load, it still has higher overall efficiency because it only processes a small fraction of the output power. This effect can be improved through selection of the supplemental converters for the correct output power ratio.

Table 1
Table of efficiency data

	Post-Regulated Output				Yeaman Topology				
V_{IN} AC	119.89	119.63	240.33	240.20	119.90	119.66	240.34	240.23	V_{RMS}
I_{IN} AC	1.657	3.182	0.825	1.582	1.650	3.142	0.825	1.561	I_{RMS}
Power Factor	0.926	0.957	0.919	0.948	0.926	0.955	0.917	0.949	---
Pin System	**183.96**	**364.29**	**182.21**	**360.24**	**183.20**	**359.05**	**181.82**	**355.87**	W
P_{OUT_ACFE}	169.98	336.79	169.85	336.87	169.16	333.30	169.32	332.78	W
V_{IN_PRM}	48.48	48.04	50.99	52.10	5.56	5.96	5.49	5.90	V_{DC}
P_{IN_PPP}	169.77	335.87	169.66	336.19	22.43	42.62	22.00	42.07	W
V_{OUT_SYSTEM}	54.07	54.06	54.06	54.06	54.00	54.00	54.00	54.00	V_{DC}
I_{OUT_SYSTEM}	3.02	6.02	3.02	6.02	3.03	6.03	3.03	6.03	A_{DC}
P_{OUT_SYSTEM}	163.46	325.65	163.44	325.66	163.41	325.49	163.40	325.48	W

	Per-Unit Efficiencies				System Efficiencies			
AC FE	92.40%	92.45%	93.22%	93.51%	92.34%	92.83%	93.12%	93.51%
Post Regulator	96.28%	96.96%	96.33%	96.87%	74.96%	84.22%	75.54%	84.51%
System	88.86%	**89.39%**	89.70%	**90.40%**	89.20%	**90.65%**	89.87%	**91.46%**

The efficiency calculated by the Vicor PowerBench™ whiteboard was 97.42% and 85.61% at full load for the post-regulated and Yeaman Topology configurations, respectively. That is not a bad estimate considering that it did not take into account the AC ripple nor interconnection losses.

Output-line ripple rejection performance

The purpose of this exercise, of course, is not to re-regulate the output; it is to reduce the line ripple voltage. Figure 9 shows the output ripple both before and after the regulator stage:

Figure 9
Post-regulated output line frequency ripple and spectra

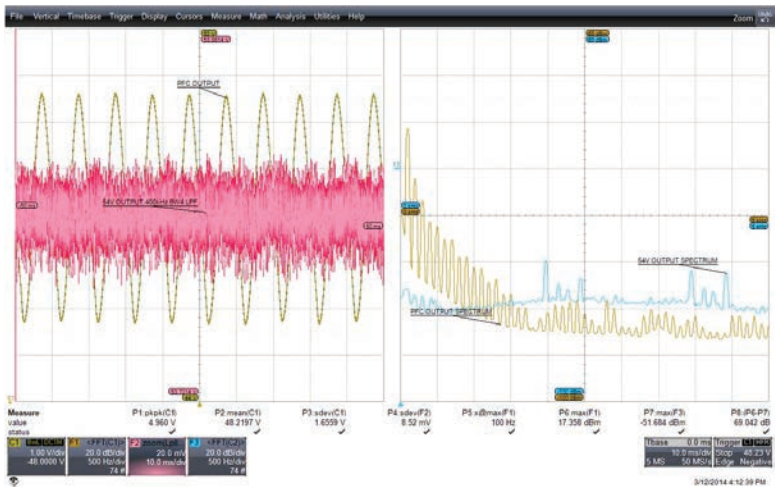
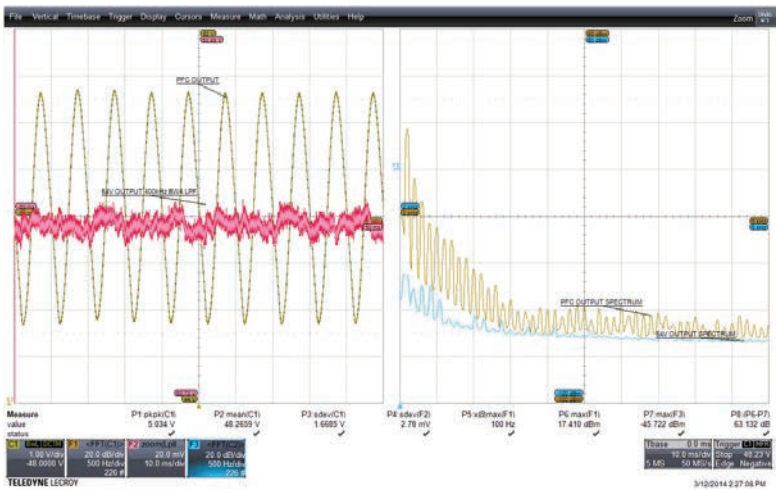


Figure 10
Yeaman Topology output line frequency ripple and spectra



The Yeaman Topology output has reduced the output ripple from $1.67V_{RMS}$ to 2.78mV. It has reduced the 100Hz component by 63.1dB

The post-regulated topology has done a better job, reducing the 100Hz ripple by 69dB. It has a noisier output, however, with $8.52mV_{RMS}$ of noise (400kHz BW limited), with local peaks at 2kHz and 3.9kHz. The reason the Yeaman Topology is quieter is because of the extra stage of galavanic isolation.

References

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