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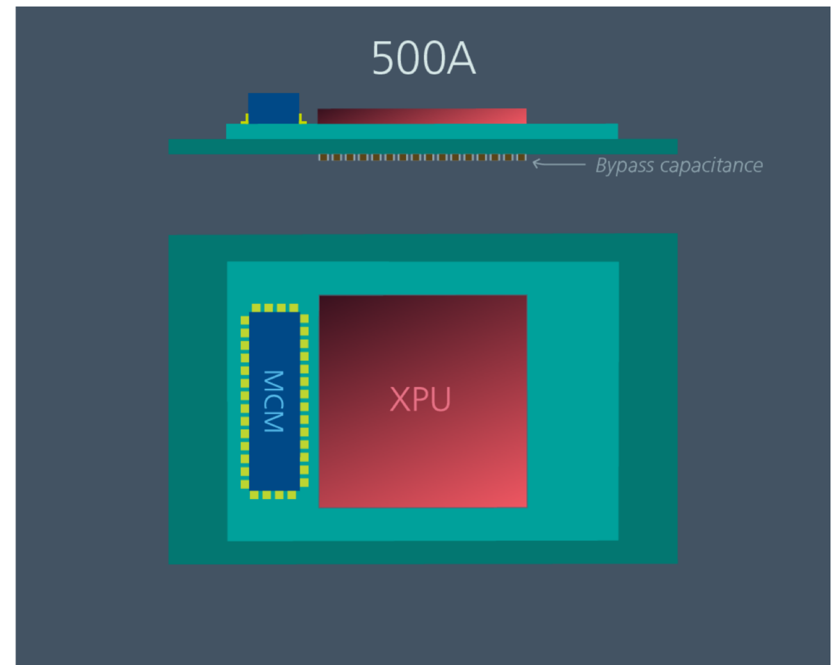
The Future of Power Integrity

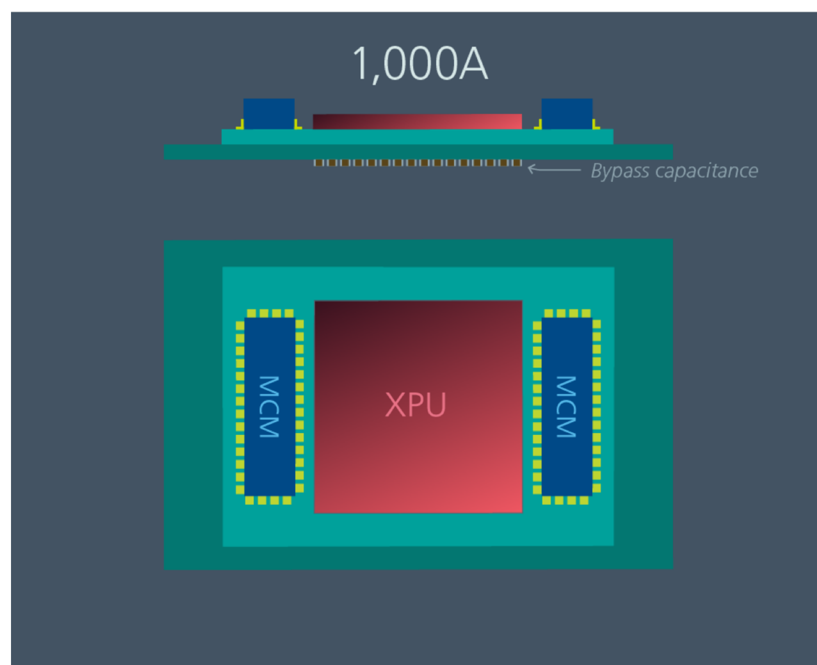
DesignCon 2019

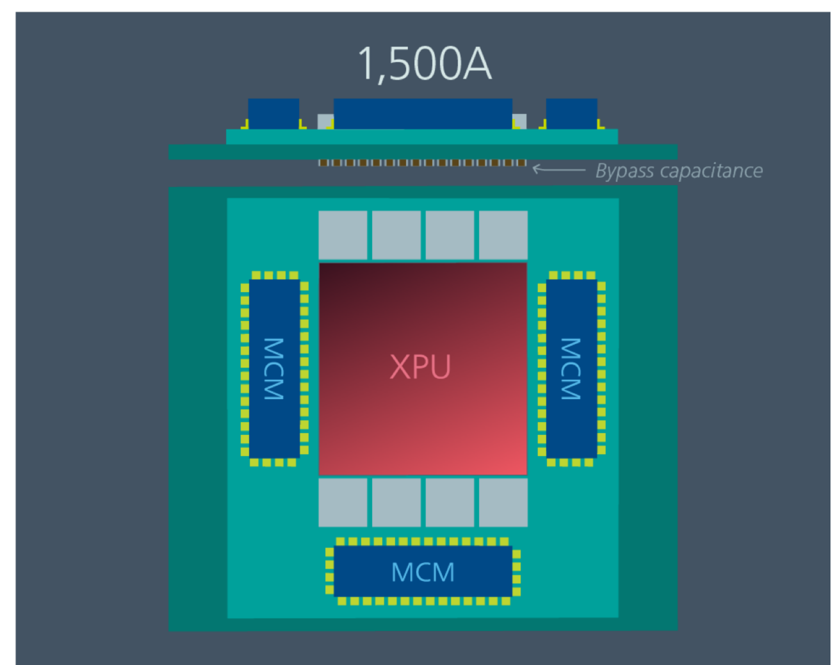
VICOR

Present: Lateral Power Delivery from XPU sides

- **Current Multipliers ("MCMs")**
  - Current density: 1.2A/mm^2
  - Interconnect resistance: 100μΩ per XPU side
- **Lateral power delivery issues:**
  - PDN loss
  - PDN impedance
- **Access to XPU constrained by PDN**
  - HBM
  - HDI







Future: Vertical Power Delivery accelerates XPU performance

- **Geared Current Multiplier (“GCM”)**
  - X&Y array of cells fits within the XPU footprint
  - Low interconnect resistance (e.g., 10μΩ)
  - Terminal pitch matched to XPU (e.g., 1mm)
  - XPU perimeter unobstructed
- **Power integrity**
  - Bypass capacitors re-located within the GCM
  - Low GCM output inductance (e.g., 3pH)
  - Low noise ZCS/ZVS current multiplication
- **Easier to cool**
  - Vertical PDN loss much lower than Lateral PDN
  - Relatively low GCM heat load
  - GCM components: ceramics and LV FETs
  - GCM cells capable of high temp operation