Meeting Transient Specifications for Electrical Systems in Military Vehicles

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Introduction

Electrical systems in military vehicles are normally required to meet stringent transient requirements. Typical of these specifications is the MIL-STD-1275B. Although the specified levels of these surges and spikes are outside the capability of Vicors Maxi, Mini, Micro Series modules, it is quite possible, with simple circuitry, to make the 24V input (18 – 36V input range) DC-DC converter modules compliant to these specifications for the 28V vehicle voltage system. Other electro-magnetic compatibility requirements, such as MIL-STD-461E and/or DEF-STAN 59-41, apply to military vehicles, but these are outside the scope of this application note. In order to meet additional conducted emission requirements an input filter, preceding the transient protection circuit covered in this application note, will be required.

The transients on this 28V rail fall into two types:
1. Spikes: typically high voltage rise, short duration and low energy.

2. Surges: typically lower voltages rise, long duration and high energy.

Many systems are battery plus generator fed with spike and surge requirements that can be easily met using the M-FIAM5 filter and transient protection module. The level of immunity imposed by MIL-STD-1275 requires additional protection such as that presented here. Incidentally, both surges and spikes are most onerous in generator-only systems. Table 1 summarizes the worst-case spike and surge requirements for the two specifications.

Table 1
Worst-case Transient Requirements

	MIL-STD-1275B	DEF-STAN 61-5
Spikes	Amplitude ±250V 50µs spike width in a burst up to 1ms duration with 15mJ maximum energy content per spike	Amplitude +270V & -220V 10µs max. Plus +110V train of spikes lasting up to 5ms
Surges	100V for 50ms from a 0.5Ω source impedance, repeated 5 times once per second	100V (+5/-0%) for 50ms from a 0.55Ω source impedance, repeated 5 times once per second (Annex C)

Note: Low line dips to 15V specified in the above specifications are likely to result in the DC-DC converter module turning off during this period. Cranking voltages will also activate the undervoltage lock out.

To protect the power converter module from these transients, two separate techniques must be used. For spikes, a parallel transient filter, e.g., input TransZorbs®, can easily remove these low energy high voltage bursts. Three P6KE33A should be placed in series and connected across the input rail, but a single 1.5KE100A could be an adequate alternative for spike removal. For surges, because of their duration and energy, the only feasible removal method is a series surge suppression circuit, i.e., a properly controlled power semiconductor(s) is/are placed in series with the input line. Since the 24V modules have a maximum input voltage of 36V, the ideal surge protection circuit would allow current to be supplied to the load module,while dropping the excess voltage associated with a surge event. The series pass element must dissipate the power associated with the excess voltage and load current. Large loads require significant power handling capability. The most suitable device for this application is a MOSFET. A BJT could also be used, but during normal operation a 0.5 – 1V drop across this device would have to be tolerated.

Circuit Description and Operation

Figure 1 is a diagram of a transient/surge protection circuit. High voltage, low energy spikes are absorbed by the capacitor and TransZorb®s across the input. All of the remaining circuitry addresses the problem of high energy surges by performing two functions. (1) The output is clamped at 35V in the event that the input rises beyond that point. (2) If the overvoltage condition at the input persists for a period greater than 55ms, the converter is shut down via the PC pin.

A charge pump provides full enhancement gate bias to the MOSFET (Q1) during normal operation. This function is accomplished by U1, an ICM7555 timer, which generates a rectangular waveform at 109kHz, that is peak detected and level shifted by R3, C4, D1 & D3. Capacitor C7 limits the rate of rise of the voltage across the output to 160 – 170V/ms, which in turn, limits the inrush current at start up to 3.5A with a 1000µF (C5) capacitor across the output. The V24 series of modules employ undervoltage lockout at approximately 16V, and a soft start feature. Start up takes longer than 10ms after crossing the lockout threshold. Zener diode D5 limits the maximum voltage that can be applied to the gate of the transient protection MOSFET to 15V, with respect to its source. If the input voltage exceeds 35.3V_{DC}, this circuit performs as a series pass linear regulator. The output voltage is compared with the LM10's reference voltage (1.95V). The error signal at the output of the LM10 is used to control transistor Q2 (2N5550), causing FET Q1 (IXTH75N10) to act as a voltage regulator. Capacitor C6 is the main spike removal device (the TransZorbs are only for added protection). C6 can also help reduce any high frequency ringing that may be applied to the circuit, although a small damping resistor in series with this capacitor may be required if the TransZorbs are not to be relied upon. D4 is added to limit the maximum voltage on C7, at high line, that may slow down the response time of this circuit. Usually, this protection circuit should be placed after the system's EMI filter, because a differential source inductance of at least 10µH is recommended to ensure that Q1 is not over stressed during high slew rate events. Differential inductance in excess of this value is also required to meet military EMI requirements. The value of C5 is dependent on the module and the application, but it must not exceed 1000µF for this circuit. Normally, 330µF is a large enough input capacitor for a single module.

In the circuit of Figure 1 power handling is limited by FET Q1, particularly during the surges.A brief explanation of the theoretical handling capability of this MOSFET is given in the appendix. In short, this MOSFET, provided its case temperature is kept below 70°C, will provide protection for a 125W load (a single V24 100W micro module, fully loaded) during a 100V surge lasting 50ms. A simple additional circuit, shown in Figure 2, can provide extra system protection in the event of a sustained overvoltage condition. If a surge lasts longer than about 50 – 60ms, or repeats faster than once per second, this circuit will turn off the attached module. Because the power dissipated in the MOSFET is proportional to loading of the transient protection circuit, it will withstand 100V surges, in the unloaded condition, almost indefinitely. This additional protection should be employed in most applications.

Figure 1
Transient Protection Filter Circuit

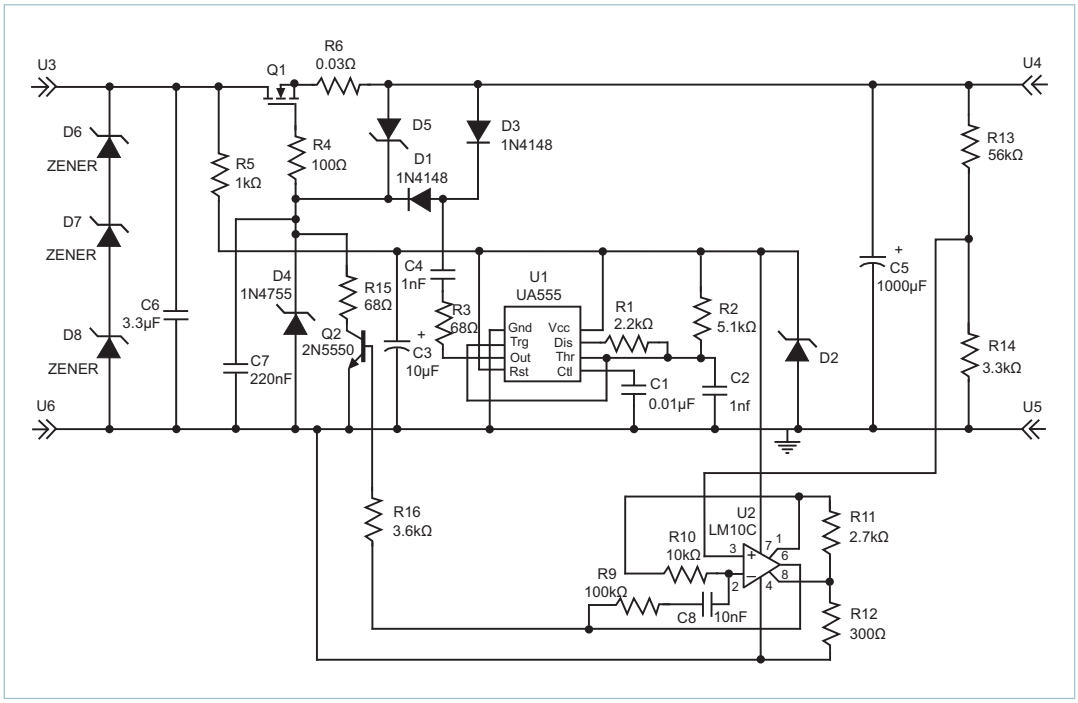
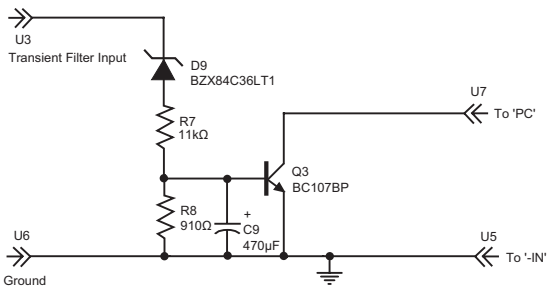


Figure 2
Surge Duration Protection Circuit



Low Line Operation

For the circuit of Figure 1 used at the suggested power, therewill be approximately 120mV drop due to the ON resistanceof the MOSFET. Some further allowance should also be made for the EMI filter and trace resistances. Therefore, low line performance can be improved by using larger or paralleled MOSFETs. Although the maximum undervoltage turn on voltage for 'V24' range of modules is 18.0V, they will in most instances operate (with some derating) down to 16V input, once started. Please note that many applications do not require operation during cranking but must operate down to 18.4V minimum (including ripple) for MIL-STD-1275B.

Filtering Higher Power Modules

To provide transient protection for higher power modules, e.g., Mini and Maxi modules, either MOSFETs with larger Safe Operating Areas (SOAs), or arrays of MOSFETs must be used. Presently, there is limited availability of dies of the required size to achieve the low thermal impedance required. However,many manufacturers make packaged arrays of MOSFETs for higher power applications such as the IRFK6J150 (six MOSFETs in parallel in this TO-240 package) that have a sufficiently large SOA to provide protection for a single Mini module (fully loaded) provided this HEX-pak case temperature does not exceed 57°C before the application of the surge. However, since distributors and suppliers often do not stock these parts, a custom array of MOSFETs is often the only recourse. MOSFETs will share current adequately during a surge event if the following conditions are met.

a. All the MOSFETs in the array are of the same type and ideally from the same production batch.

b. All the MOSFETs in the array are thermally coupled to the same heat sink, (i.e., all the MOSFETs need to have the same device temperature).

c. All the MOSFETs in the array have their own gate resistor, (i.e., each MOSFET must have its own 22-100Ω, R4 resistor).

d. Drain, gate and source, current traces should be of similar lengths and impedance.

e. A small source resistor R6 can be added for improved MOSFET current sharing, if required.

A discussion of the reasoning behind these criteria is given in the Appendix & Notes section. Under the above ideal circumstances, sharing should be very accurate; however, because points (a) and (b) are unlikely to be always met, some degree of derating is advisable. Table 2 shows the suggested power handling capability of the IXTH75N10 at 50°C, 60°C, 70°C & 80°C case temperatures.

Table 2
IXTH75N10 Power Handling vs. Case Temperature.

Case Temperature	Q1	Q1 x2	Q1 x3	Q1 x4
50°C	163W	288W	403W	500W
60°C	144W	250W	346W	424W
70°C	125W	212W	289W	348W
80°C	106W	174W	232W	272W

Note: Greater reliability will be achieved by having individual transient protection tailored for each module in a power application.

Appendix and Notes

Table 3
Bill of Materials for the Circuit Shown in Figure 1

Circuit Reference	Part Number	Description & Notes
U1	ICM7555	CMOS 555 Timer (Intersil)
U2	LM10CN	Op Amp & band-gap reference
Q1	IXTH75N10	100V 75A Power MOSFET (IXYS)*
Q2	2N5550	NPN Epitaxial BJT (Fairchild)
Q3	BC107B	NPN BJT (Philips)
D1	1N4148	Silicon signal diode
D2	BZX85C12	12V Zener (1.3W)
D3	1N4148	Silicon signal diode
D4	1N4755	43V Zener
D5	1N5245	15V Zener
D6	P6KE33A	TransZorb (600W)
D7	P6KE33A	TransZorb (600W)
D8	P6KE33A	TransZorb (600W)
D9	BZX84C36	36V Zener
C1		Capacitor MF 10nF (63V)
C2		Capacitor MF 1nF (63V)
C3		Capacitor 10µF (16V)
C4		Capacitor MF 1nF (63V)
C5		Module input capacitor 220µF – 1000µF
C6		Capacitor MF 3.3µF (100V)
C7		Capacitor MF 220nF (63V)
C8		Capacitor MF 10nF (63V)
C9		Capacitor 470µF (6.3V)
R1		Resistor 2.2kΩ (0.125W)
R2		Resistor 5.1kΩ (0.125W)
R3		Resistor 68Ω (0.125W)
R4		Resistor 100Ω (0.125W)*
R5		Resistor 1kΩ (2W) Metal Oxide
R6		Resistor 30mΩ (2.5W) Metal Oxide**
R7		Resistor 11kΩ (0.4W)
R8		Resistor 910Ω (0.125W)
R9		Resistor 100kΩ (0.125W)
R10		Resistor 10kΩ (0.125W)
R11		Resistor 2.7kΩ (0.125W)
R12		Resistor 300Ω (0.125W)
R13		Resistor 56kΩ (0.125W)
R14		Resistor 3.3kΩ (0.125W)
R15		Resistor 68Ω (0.125W)
R16		Resistor 3.6kΩ (0.125W)

* Additional MOSFETs and gate resistors are needed for higher power requirements, e.g., four for applications that use a 400 Watt converter module.
** Only for use with parallel MOSFETs applications when sharing is poor.

MOSFET Safe Operating Area (SOA)

The power handling capability of a device such as a MOSFET is referred to as the safe operating area for that device. A typical graph is shown in Figure 3.

More informative data can be often obtained from the transient thermal impedance data for the device in question. From this information the power handling of a particular MOSFET at a particular die temperature can be determined. Generally, the SOA data is available only at 25°C junction temperature. Transient thermal impedance data (see Figure 4) can be used to calculate the safe initial temperature of the MOSFET, for a given pulse of defined energy.

Figure 3
SOA Curve for an IXTH75N10

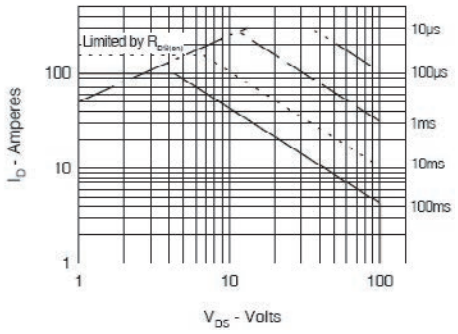
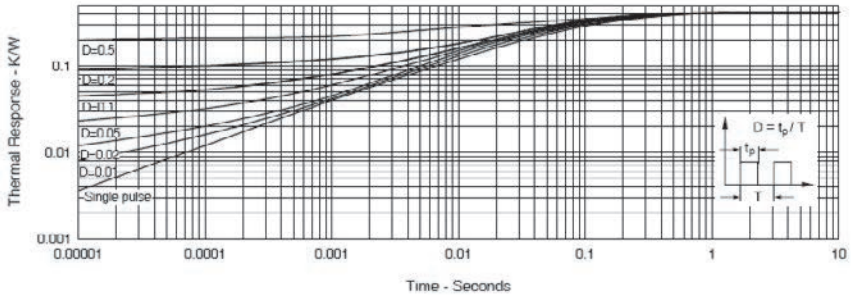


Figure 4
Transient Thermal Impedance



For example an IXTH75N10 with a 0.05 duty cycle (50ms in 1sec) has a transient thermal impedance for a 50ms pulse of about 0.28°C/W. Therefore if a current of 3.5A is flowing through a single MOSFET during a 100V surge (of which 35.3V appears across the module, provided the surge protection circuit above is used) the expected die temperature rise is estimated at:

$$\Delta T = 63.4°C = (100V - 35.3V) \bullet 3.5A \bullet 0.28°C/W$$

Since this MOSFET has a maximum operating junction temperature of 150°C (some manufacturers claim higher maximum junction temperatures[1]) this limits the maximum temperature, at the start of the surge to 86°C. A further rise of 5°C is to be expected due to the 5 repeated surges, limiting the maximum initial die temperature to 81°C. This is the reason for the recommended maximum starting case temperatures in the text. The recommended maximum also allows for a suitable safety margin, plus the normal conduction dissipation temperature rise, of the die junction above case, occurring prior to the surge.

Note: A larger C5 value can also reduce the SOA, as C5 is rapidly charged at the beginning of a surge to 35.3V, resulting in extra MOSFET dissipation.

Expanding Power Handling

Ideally choosing a larger MOSFET is the best solution for higher power applications, but these are often not available, so the alternative is to parallel MOSFETs. MOSFETs will approximately share load current provided the requirements for points (a) & (b) in the above text are adhered to[2][3][4]. Arrays of MOSFETs need individual gate resistances (c) to prevent high-frequency oscillation, particularly when used in a linear mode[5]. Normally, a value of between 22 – 100Ω is recommended; however, for this application, because fast charging of the module input capacitance is not required and may result in detrimental system reliability, a 100Ω resistor is more appropriate. A 100Ω resistor may reduce the requirement for circuit input impedance as well. Besides point (d) being good engineering practice, it will help to ensure that the instantaneous voltages applied to the gate of each MOSFET are similar.

The choice of R6, point (e), should ideally be:

$$R6 > 1/g_m \; Therefore, R6 > 1/25 = 0.04\Omega \; for \; the \; 1XTH75N10$$

The larger the resistance of R6, the better the current sharing, but at the expense of dissipation and low line operation[3]. For example, a value of 100mΩ would result in about a 0.7V drop across the filter during low line dips. That may not be acceptable given the operating range of the Vicor 2nd Generation 24V input modules. Furthermore, each resistor would dissipate about 2W typically. However, as the waveforms below show, even a much smaller value of MOSFET source resistance can help. R6 between 30 – 50mΩ seems to be quite a good compromise with the IXTH75N10 in this application, but this device should not be necessary if a well-laid-out design is used.

Waveforms & Data

Note: A mechanical switch in series with a 100V source was used to simulate the surge.

Figure 5
Turn On Characteristics at 400W load.
***CH1** = '24' Module Input voltage*
***CH2** = Input Current 1275 Filter. 5A/div.*
Four IXTH75N10 in parallel

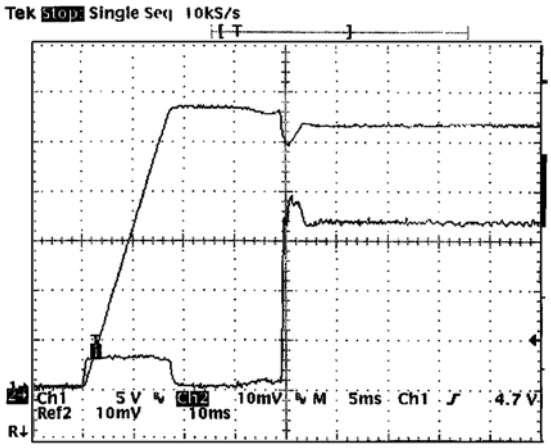


Figure 6
Surge Performance
***CH1** = Voltage Applied to Filter*
***CH2** = Voltage Applied to V24A28C400AL at Full Load*

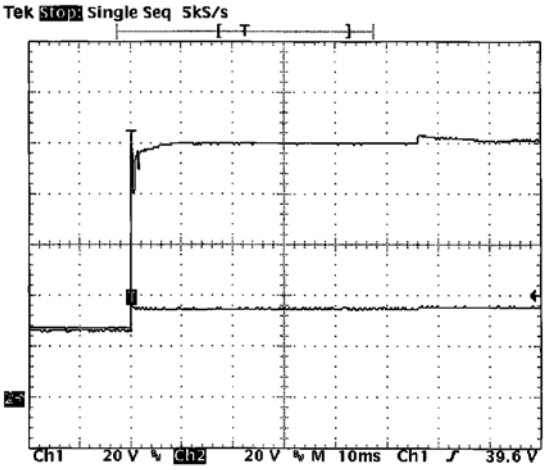


Figure 7
Surge Performance
(Faster Timebase)
CH1 *= Voltage Applied to*
V24A28C400AL at Full Load.
CH2 *= Voltage Applied to Filter*

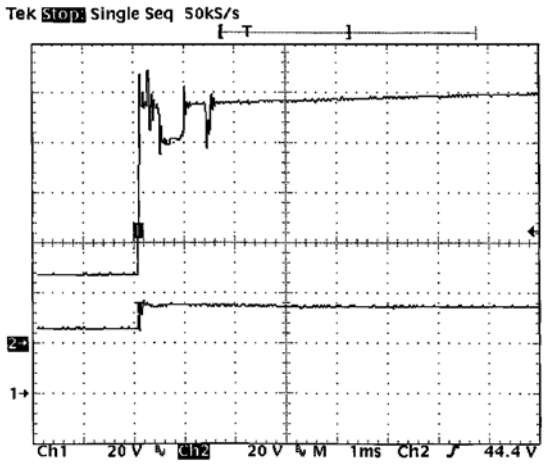


Figure 8
Input & Output Voltage
(Surge End 70W Load).
CH1 *= Voltage Applied to*
V24A28C400AL.
CH2 *= Voltage Applied to Filter*

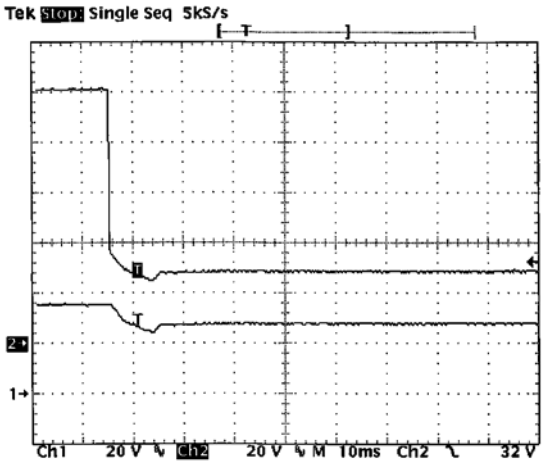


Figure 9
Surge PC Voltage
CH1 *= Input to 1275 Filter*
CH2 *= PC Pin Voltage*
During Surge

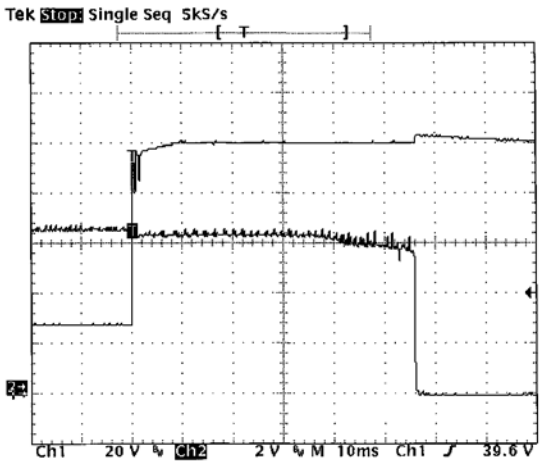


Figure 10
Input & Output Characteristics
CH1 *= Input to 1275 Filter*
CH2 *= V24A28C400A Output Voltage at Full Load*

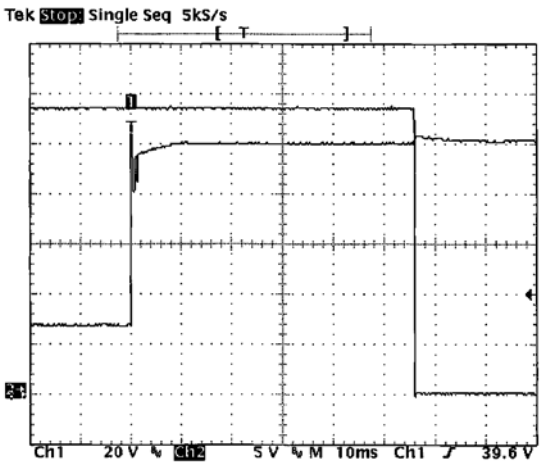


Figure 11
Input Current & Voltage
CH1 *= Input to 1275 Filter*
CH2 *= Input Current to Filter at Full Load 5A/div*

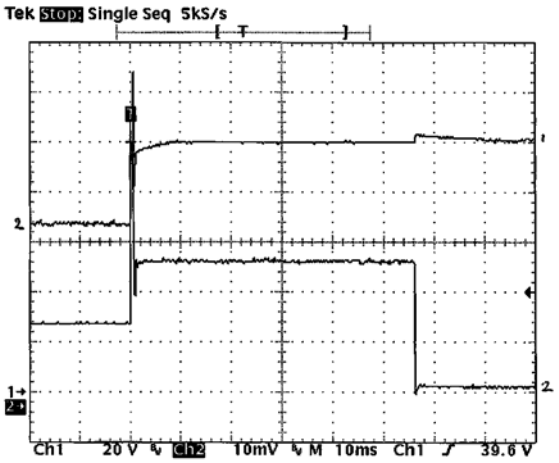


Figure 12
Module Input Voltage & System Current
CH1 *= V_{IN} for V24A28C400A*
CH2 *= Filter input current 17 – 13A (5A/div)*

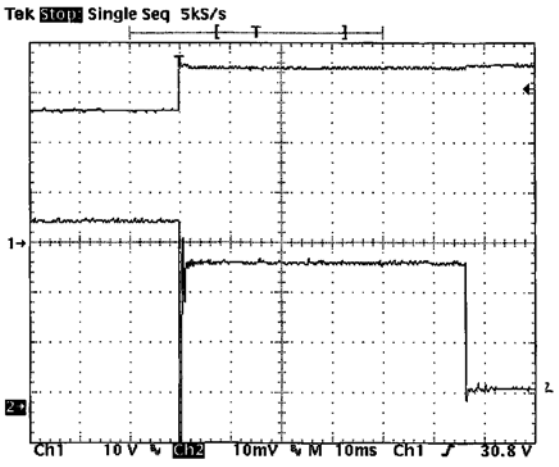


Figure 13
FET 1 Current & Module V_{IN}
***CH1** = V_{IN} of V24A28C400A (Full Load)*
***CH2** = FET 1 Current 2A/div*

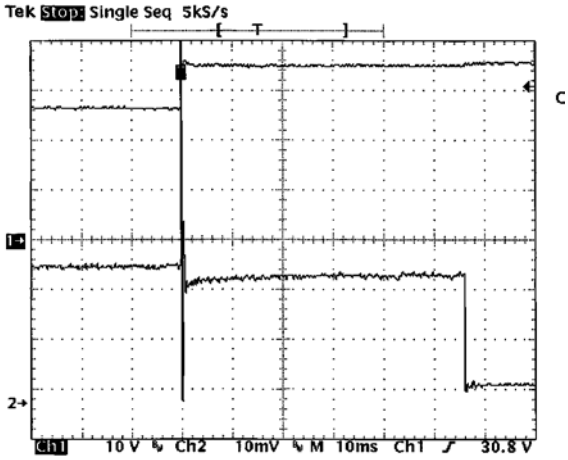


Figure 14
FET 2 Current
***CH1** = V_{IN} of V24A28C400A (Full Load)*
***CH2** = FET 2 Current 2A/div*

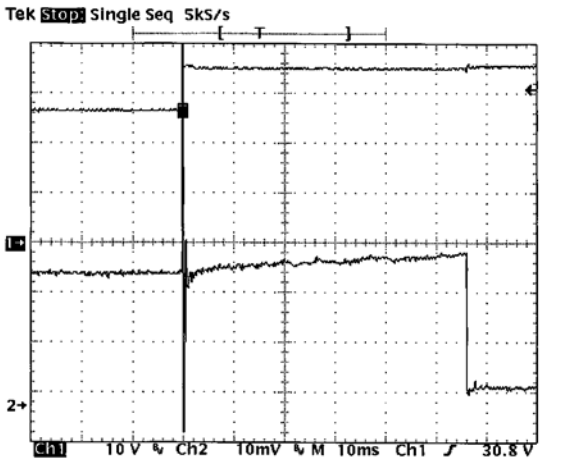
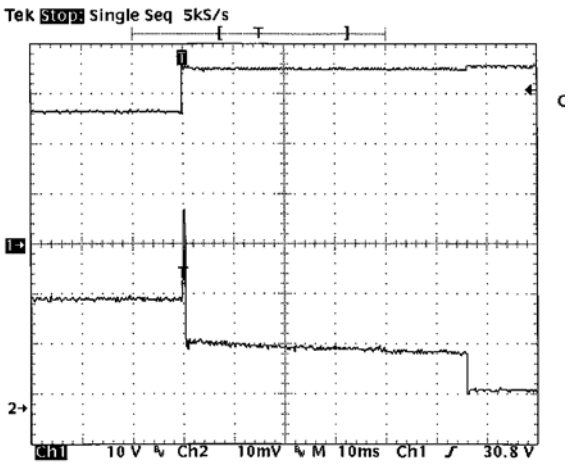
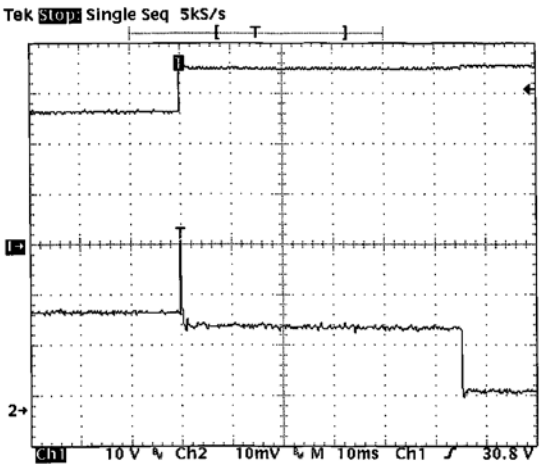


Figure 15
FET 3 Current
***CH1** = V_{IN} of V24A28C400A (Full Load)*
***CH2** = FET 3 Current 2A/div*



Note: FET 3 & 4 were laid out some distance from FETs 1 & 2 to show typical performance degradation.

Figure 16
FET 4 Current
CH1 *= V_{IN} of V24A28C400A (Full Load)*
CH2 *= FET 4 Current 2A/div*



Effect of adding an individual 30mΩ source resistance to each MOSFET.

Figure 17
Effect of 30mR. FET 2 Current
CH1 *= V_{IN} of V24A28C400A (Full Load)*
CH2 *= FET 2 Current 2A/div*

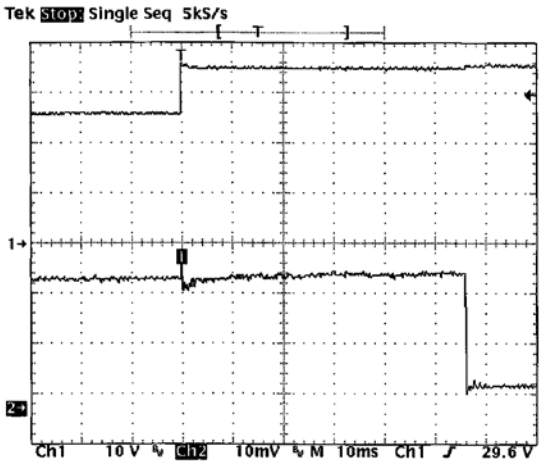
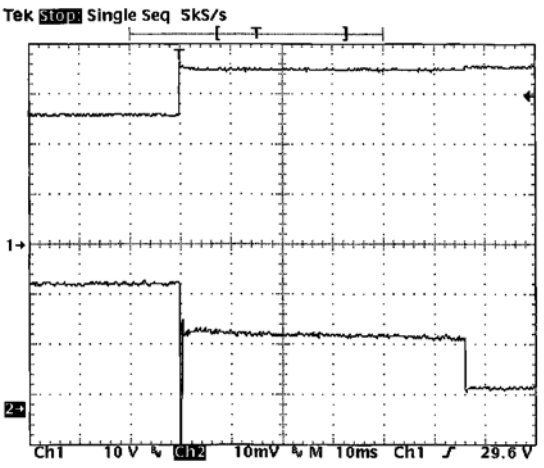


Figure 18
Effect of 30mR. FET 3 Current
CH1 *= V_{IN} of V24A28C400A (Full Load)*
CH2 *= FET 3 Current 2A/div*



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[2] MOSFET Linear Operation by Mark Alexander.
[3] Parallel Operation of Power MOSFETs by Rudy Severns
[4] Thermally Forced Current Sharing in Paralleled Power MOSFETs by John G. Kassakian.
[5] An Analysis and Experimental Verification of Parasitic Oscillations in Paralleled Power MOSFETs by David Lau (from IEEE Transactions on Electron Devices,Vol. ED-31 No.7 July 1984).

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