Micro DC-DC Converter Family
Isolated Remote Sense

Application Engineering
Vicor Corporation

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Introduction

The Vicor Brick Micro DC-DC converters do not have remote-sense pins. Nevertheless, remote sense can be achieved by employing external circuitry. A circuit is proposed that senses the voltage at the load and adjusts the converter output voltage to compensate for the voltage drop in the leads / traces. It also provides isolation of the sense leads / traces that is beneficial in high-noise applications.

Design Considerations

DC Considerations

The Vicor Micro module's output can be trimmed up to a maximum of 10% over the nominal output voltage. This limits the amount of lead / trace resistance the isolated remote-sense circuit can correct for. Maximum round-trip lead resistance at full load is governed by the following formula:

$$R_{LEAD\_MAX} = \frac{1.1 V_{OUT\_NOM} - V_{POL}}{0.9\, I_{MAX}} \qquad (1)$$

V_{OUT_NOM}:   Nominal output voltage of the converter

V_{POL}:   Voltage at the point of load

I_{MAX}:   Converter rated output power ÷ V_{OUT_NOM}

Note: As the module output voltage is trimmed up, the output current drawn from the module must be reduced proportionally. This is why I_{MAX} is multiplied by 90% when the module is trimmed up 10%.

The proposed circuit may cause oscillation with large output capacitance at light loads. A minimum load of 10% of the maximum is recommended.

AC Considerations

As the load is moved further away from the output of the converter, lead / trace impedance will increase. Since the Micro module has local sensing at the output terminals, this impedance causes the voltage that the converter regulates to be different from the voltage seen by the load.

This remote sense circuit solves this problem by putting the lead / trace impedance inside the control loop of the converter. Figure 1 shows a very lossy distribution network between the converter and point-of-load.
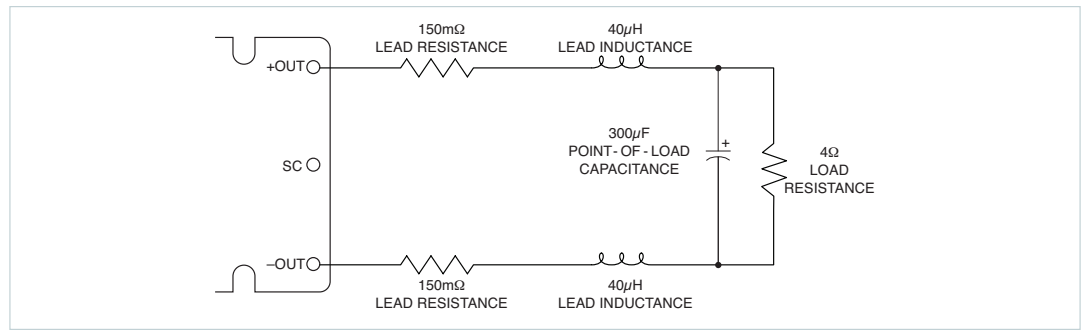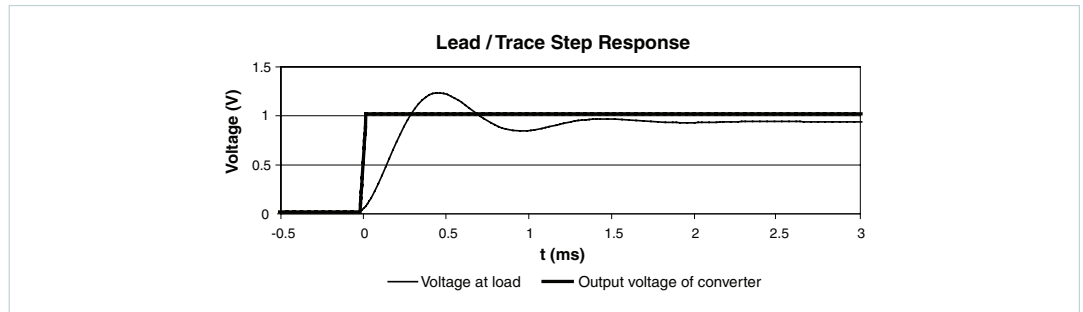
Figure 2 illustrates the effect of this parasitic network in the time domain. The step response shows the point-of-load voltage is delayed with respect to the converter output. This limits how fast the converter can correct for voltage changes at the load.

In the frequency domain this delay results in phase shift that increases with frequency. This is demonstrated by the Bode plot of this network shown in Figure 3.
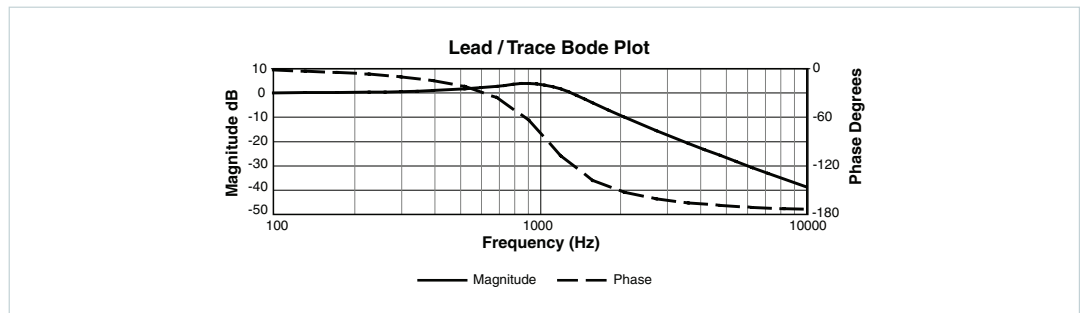
Whenever phase shift is introduced into a control network, the stability of that loop will be degraded. This occurs because the control loop is trying to correct for conditions that have already occurred. As phase shift approaches –180°, the control loop falls so far behind that the system will begin to oscillate. This consideration will always be an issue when remote sense is used, regardless of whether it is realized with built-in sense leads or an external circuit.

To prevent instability, the designer must reduce the loop gain below unity before phase shift becomes significant. This leads to a fundamental trade off in control system design because reducing the system bandwidth will degrade its transient response.

Figure 4
Model of the SC Pin
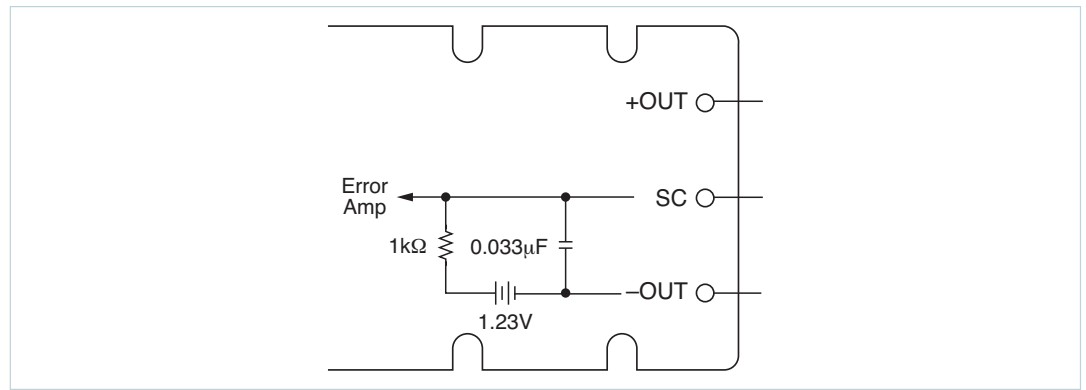
Remote-Sense Circuit Functional Description

As shown in Figure 5, an op-amp with a built-in precision reference (U3) maintains voltage regulation at the point-of-load. The reference voltage is scaled up from 200mV with the external-resistive network formed by R7 and R8 to 1.245V. The reference has a compensation capacitor (C2) that slows the ramp-up time to control turn-on overshoot.

The op-amp compares this reference voltage to the point-of-load voltage scaled by R9 and R10. The output of the op-amp drives the cathode of an optocoupler (U1). The optocoupler isolates noise voltages that are present at the negative-output lead thereby keeping them from appearing on the SC pin. The speed at which the external loop can respond to load transients is determined by the compensation capacitor (C3) and the parallel combination of the voltage-sensing resistors (R9 and R10). R11 allows C3 to fully discharge when power is removed from the circuit.

The optocoupler is connected to the SC pin via resistors R1 and R2. These resistors program the maximum output voltage at the converter (R1) and the minimum-output voltage of the converter (R2). Figure 4 shows how the internal connections of the SC pin form a RC filter that will limit overall system bandwidth.

The op-amp and the optocoupler are both powered from the output of the converter via a shunt regulator (U2) that is programmed to provide a 2V rail.

Figure 5
Circuit Schematic
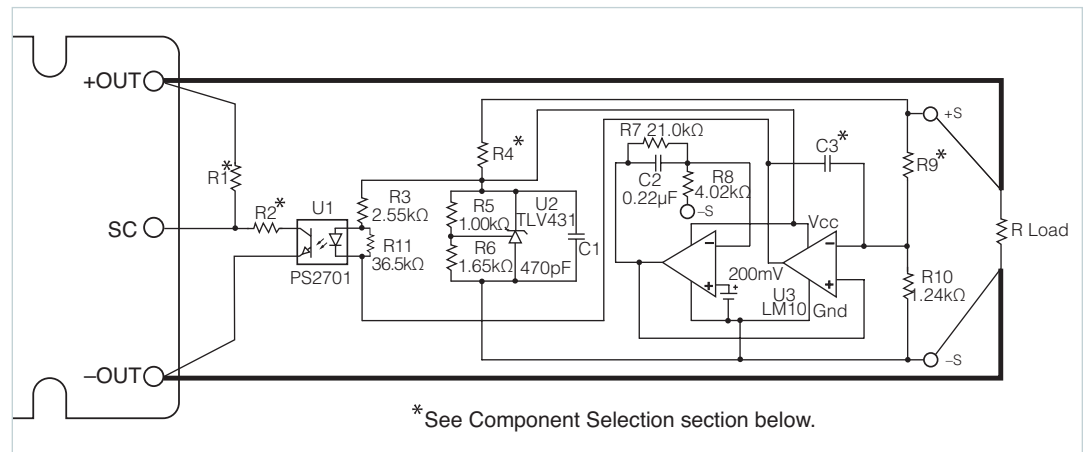
Component Selection

Table 1 gives resistor values for some common output voltages. For applications that are not listed, formulas for calculating resistor values are also given.

V$_{OUT\_NOM}$ (V)	V$_{OUT\_MAX}$ (V)	V$_{OUT\_MIN}$ (V)	R4 (kΩ)	R1 (kΩ)	R2 (kΩ)	R9 (kΩ)
3.3	3.63	2.97	0.091	18.7	3.57	2.05
5	5.5	4.5	0.2	34.0	3.57	3.74
8	8.8	7.2	0.39	60.4	3.57	6.65
12	13.2	10.8	0.68, 0.5W	95.3	3.57	10.7
15	16.5	13.5	0.82, 0.5W	124	3.57	13.7
24	26.4	21.6	1.5, 0.5W	205	3.57	22.6
28	30.8	25.2	1.8, 1.0W	237	3.57	26.7
36	39.6	32.4	2.2, 1.0W	309	3.57	34.8
48	52.8	43.2	3.0,1.0W	422	3.57	46.4

All resistors are ¼W unless otherwise specified.

V$_{OUT\_NOM}$: Nominal output voltage of the converter and point-of-load voltage

V$_{OUT\_MAX}$: Maximum output voltage of the converter that supplies the load and lead / trace loss

V$_{OUT\_MIN}$): Minimum output voltage of the converter typically set to 90% of V$_{OUT\_NOM}$

Solving for R1

The value of R1 is governed by the following formula:

$$R1 = 1\ k\Omega\ \frac{V_{OUT\_MAX} - 1.23V)\ V_{OUT\_NOM}}{1.23V\ (V_{OUT\_MAX} - V_{OUT\_NOM})}\ - 1k\Omega$$

Solving for R2

R2 can be calculated as follows, where VCE$_{SAT}$ is the saturation voltage of the optocoupler given by the manufacturer (0.3V for the NEC PS2701):

$$R2 = \frac{\dfrac{V_{OUT\_MIN}\ 1.23V}{V_{OUT\_NOM}} - VCE_{SAT}}{\dfrac{V_{OUT\_MIN}}{R1}\left(1 - \dfrac{1.23V}{V_{OUT\_NOM}}\right) + \dfrac{1.23V}{1k\Omega}\left(1 - \dfrac{V_{OUT\_MIN}}{V_{OUT\_NOM}}\right)} \qquad (3)$$

Solving for R4

With different module output voltages R4 will need to be changed such that current being fed into the TLV431 regulator is approximately 15mA.

The following equations can be used to find the appropriate value for R4 and its power dissipation PR4:

$$R4 = \frac{V_{OUT\_NOM} - 2V}{15mA} \qquad (4)$$

$$P_{R4} = (V_{OUT\_NOM} - 2V)\ 15mA$$

Solving for R9 and R10

The value of R10 should be 1.24kΩ to obtain a reasonable value for the parallel combination of R9 and R10. R9 can be calculated as follows:

$$R9 = R10\left(\frac{V_{OUT\_NOM}}{1.245V} - 1\right) \qquad (5)$$

Solving for C3

For good stability the bandwidth of a remote-sense circuit must be lower than the frequency where phase shift from the leads / traces becomes significant. The appropriate integrator crossover frequency can be estimated with a first-order model of the leads / traces. For many applications 200Hz makes a good starting value (C3 = 0.68μF). The optimal value will depend on design requirements. Figure 6 can be used to find C3 once the desired crossover frequency is known.

Figure 6
Crossover Frequency
vs. Capacitance

Selecting Capacitor C3
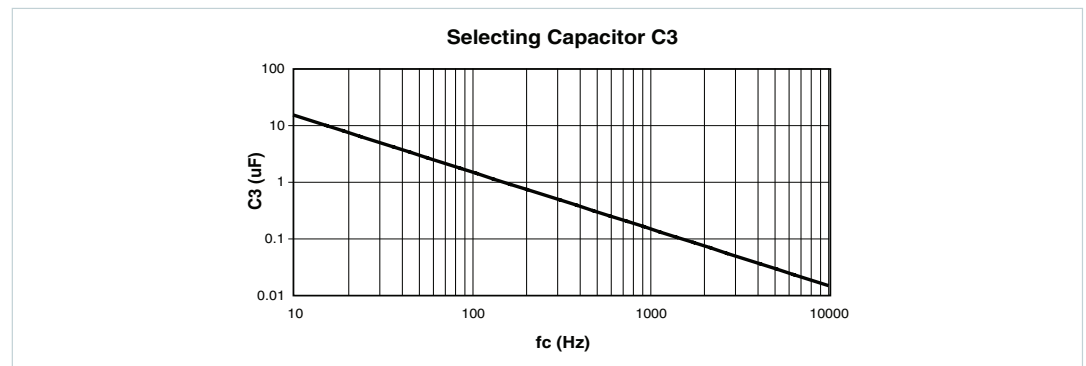
Solving for C2

C2 programs the ramp-up time of the remote-sense circuit's reference. To minimize overshoot, this should be longer than the 4ms start-up ramp of the converter (C2 = 0.22µF). The effect of changing C2 is shown in the waveforms section.

The following table gives component values for a circuit configured for a point-of-load voltage of 3.3V.

Table 2

Parts List for 3.3V Module

Ref Des	Part Description	Rating
R1	18.7kΩ	¼W
R2	3.57kΩ	¼W
R3	2.55kΩ	¼W
R4	91Ω	¼W
R5	1.0kΩ	¼W
R6	1.65kΩ	¼W
R7	21kΩ	¼W
R8	4.02kΩ	¼W
R9	2.05kΩ	¼W
R10	1.24kΩ	¼W
R11	36.5kΩ	¼W
C1	470pF	100V
C2	0.22µF	16V
C3	0.68µF	16V
U1	NEC PS2701 (Digi-Key #PS2701-1-ND)	NA
U2	TI TLV431 (Digi-Key #296-10727-5-ND)	NA
U3	National LM10 (Digi-Key #LM10CWM-ND)	NA

Circuit Waveforms

Transient Response

Figures 7, 8 and 9 show the response to a load-current step. C3 is sized for a 200Hz crossover frequency giving a clean transient response with no oscillation.

Figure 7

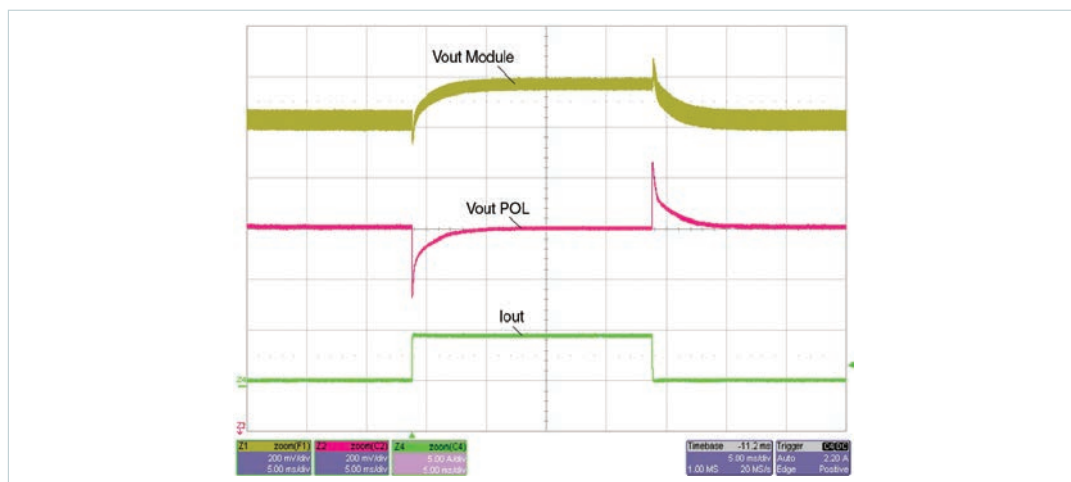*Load Step 0.5A to 5A to 0.5A, C3 = 0.64µF, 300µF at Point-of-Load (V48C3V3E75B)*

Figure 8
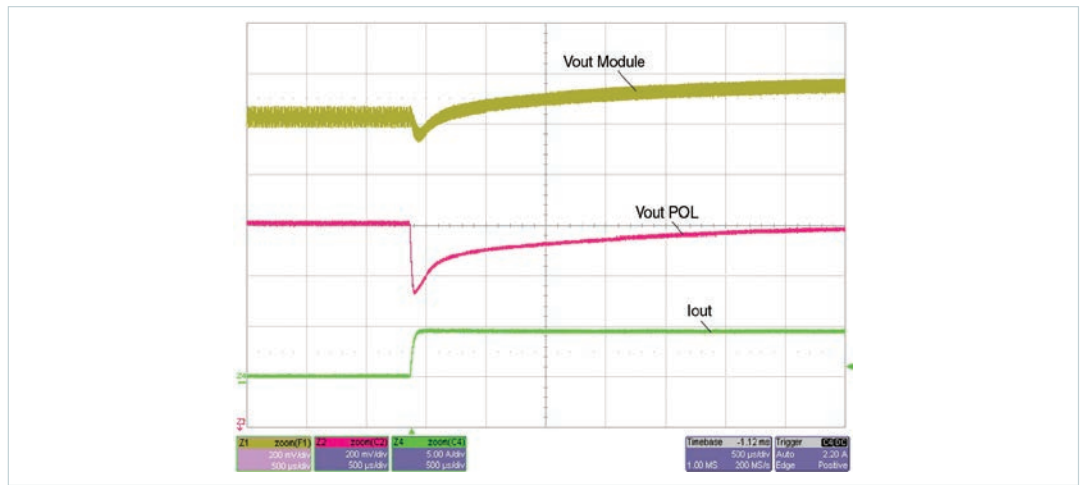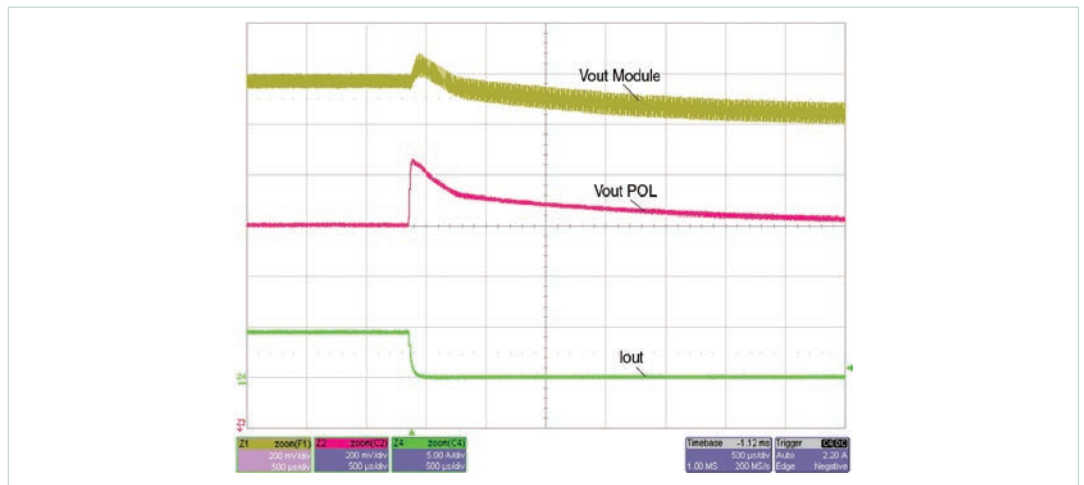*Load Step 0.5A to 5A,
C3 = 0.64µF, 300µF at
Point-of-Load (V48C3V3E75B)*

Figure 9
*Load Step 5A to 0.5A,
C3 = 0.64µF, 300µF at
Point-of-Load (V48C3V3E75B)*

Transient Response Improperly Sized C3

Figures 10 and 11 show the response to a load step with C3 undersized. They illustrate how both C3 and the point-of-load capacitance contribute to the circuit's closed-loop response.

Figure 10
*Load Step 0.5A to 5A to 0.5A,
C3 = 0.033µF, 300µF at
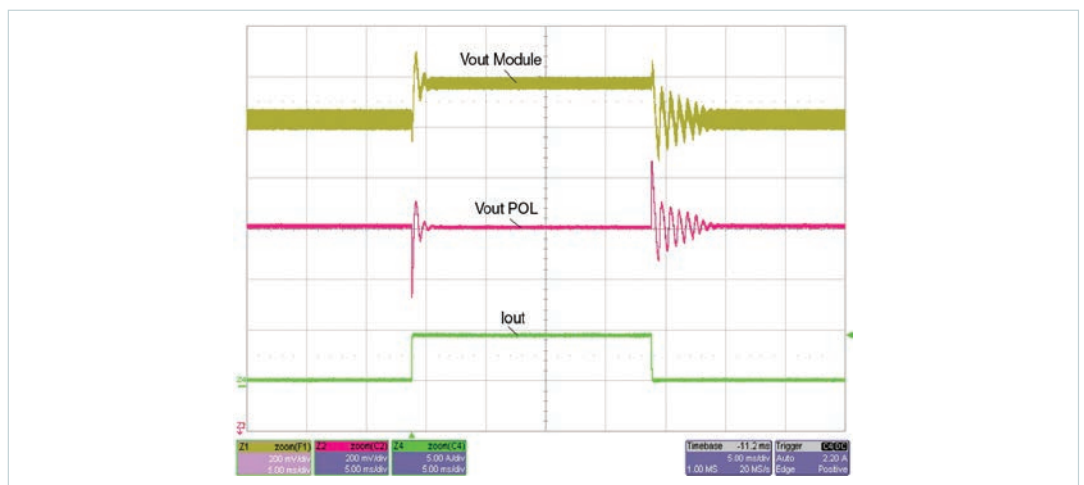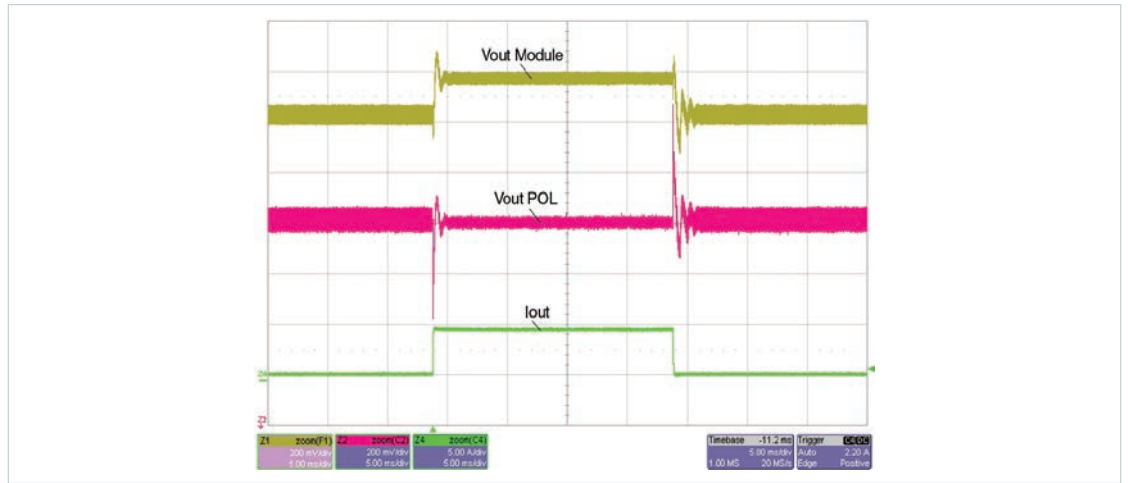Point-of-Load (V48C3V3E75B)*

Figure 11
Load Step 0.5A to 5A to 0.5A,
C3 = 0.033μF, no Point-of-Load
Capacitance (V48C3V3E75B)

Effect of C2 on Start Up

Figure 12 shows a good intermediate value for C2 which results in a reasonable start-up time and eliminates overshoot. Depending on the application, C2 may need to be resized. In Figure 13, C2 is intentionally undersized causing the reference to come up too fast and the point-of-load voltage to overshoot. Figure 14 shows start up with C2 oversized resulting in a long delay before the nominal voltage is reached.
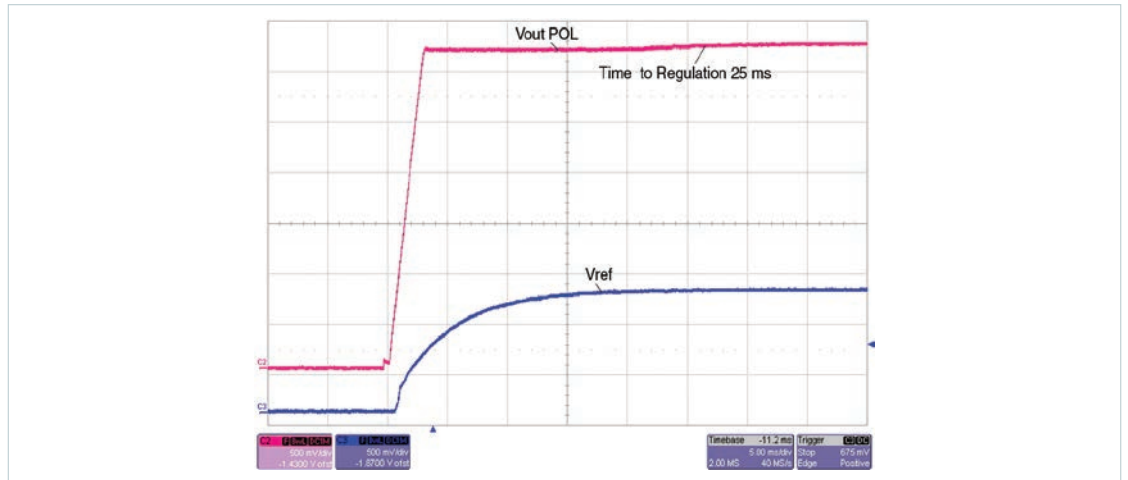

Figure 12
Start Up C2 = 0.21μF
(V48C3V3E75B)
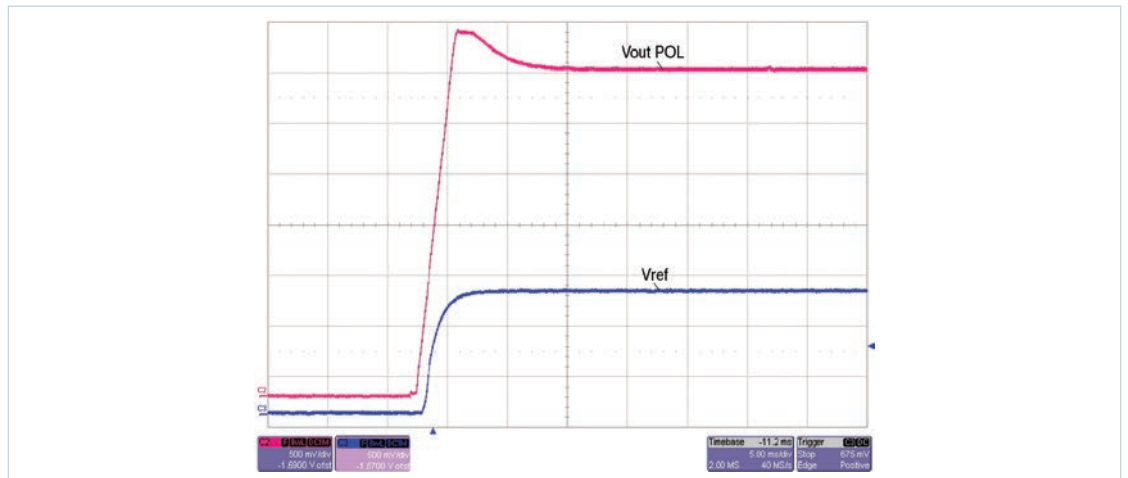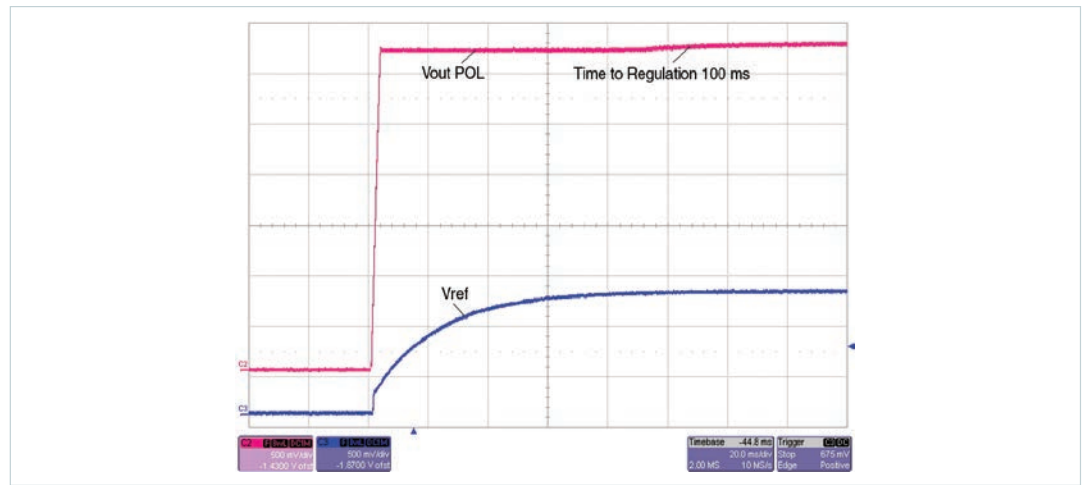

Figure 13
Start Up C2 = 0.047μF
(V48C3V3E75B)

Figure 14
Start Up C2 = 1.0μF
(V48C3V3E75B)

For more information on remote sense capabilities, please contact the Vicor Applications Engineers at http://www.vicorpower.com/contact-us for worldwide assistance.

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